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GATE ELECTRODE DOPANT ACTIVATION METHOD FOR SEMICONDUCTOR MANUFACTURING

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the invention generally relate to the field of semiconductor manufacturing processes, more particular, to methods for dopant activation within silicon-containing films forming semiconductor devices, such as gate electrodes.

Description of the Related Art

[0002] As smaller transistors are manufactured, thinner gate dielectric material is needed to enhance device performance. However, the carrier depletion contributes about 4 Å to inversion oxide thickness gate electrode material, such as p-type polysilicon doped with boron or n-type polysilicon doped with arsenic and/or phosphorous. Reducing the poly-depletion has become critical to maintain the device performance. Conventional processes include a rapid thermal annealing process which has a thermal budget limitation. For example, temperatures higher than 1050°C are undesirable since boron penetrates through the gate dielectric material to degrade device performance and reliability.

[0003] Ultra shallow source/drain junctions are becoming more challenging to produce as junction depth is required to be less than 30 nm for sub-100 nm CMOS (complementary metal-oxide semiconductor) devices. Conventional doping by implantation followed by thermal post-annealing is less effective as the junction depth approaches the size of 10 nm, since thermal post-annealing causes enhanced dopant diffusion. Dopant diffusion may contaminate nearby layers and cause failure of the device.

Activating the polysilicon gate electrode without causing dopant diffusion is a major challenge for front end of line (FEOL) processing. A tight balance exists between enhanced dopant activation and aggregated dopant diffusion. An aggressive

activation anneal may lead to high carrier concentration, but the dopant may be driven into the gate dielectric layer or even into the channel region. The balance becomes more difficult to maintain as device makers try to overcome poly-depletion. Poly-depletion is a reduction of activated dopants within the inversion region of a polysilicon layer. Poly-depletion accounts for an increasing fraction of Tox-inv (carrier concentration/poly-depletion) as gate lengths and gate dielectric thicknesses become smaller. For substrate features in the size of 130 nm and 90 nm, conventional thermal processes such as rapid thermal processing (RTP) and spike annealing are the main dopant activation methods. The resulting poly-depletion contributes 4-5 Å to Tox-inv. An additional reduction of 1 Å of the poly-depletion is necessary for a substrate feature with the size of 65 nm. Drive current gain of about 3% is expected with each angstrom of poly-depletion reduction. Conventional thermal processes are not capable of annealing such as small substrate feature without provoking dopant diffusion. In addition, preventing dopant penetration and use of thermally sensitive high-k materials requires low thermal budget activation anneal.

[0004] Laser anneal, which can achieve high dopant activation without driving dopant diffusion, has been developed to meet the requirements for poly depletion for use in 65 nm features. Laser annealing technology produces transient temperatures near the silicon melting point within a few milliseconds, which results in high dopant activation with little dopant diffusion. This is a particular benefit for a process such as boron activation, since boron diffuses much faster than does phosphorous and arsenic. However, laser anneal temperatures that melt the silicon has been shown to cause polycrystalline grain size growth which have been shown to results in device yield loss.

[0005] Therefore, there is a need to have a process for doping polycrystalline layers within a feature and subsequently annealing and activating the doped polycrystalline with minimal or no dopant diffusion.

SUMMARY OF THE INVENTION

[0006] In one embodiment, the invention generally provides a method for annealing a doped layer on a substrate including depositing a polycrystalline layer to a gate oxide layer, implanting the polycrystalline layer with a dopant to form a doped polycrystalline layer, exposing the doped polycrystalline layer to a rapid thermal anneal and exposing the doped polycrystalline layer to a laser anneal.

[0007] In another embodiment, the invention generally provides a method for annealing a layer on a substrate including depositing a polycrystalline layer containing a lattice to the substrate, doping the polycrystalline layer with at least one dopant element to form a doped polycrystalline layer and annealing the doped polycrystalline layer with a laser to incorporate the at least one dopant element into the lattice.

[0008] In another embodiment, the invention generally provides a method for annealing a doped silicon layer on a substrate including depositing a polycrystalline layer to the substrate, doping the polycrystalline layer with at least one dopant element to form a doped polycrystalline layer, exposing the doped polycrystalline layer to a rapid thermal anneal at a first temperature and exposing the doped polycrystalline layer to a laser anneal at a second temperature from about 1,000°C to about 1,415°C.

[0009] In another embodiment, the invention generally provides a method for annealing a layer on a substrate including depositing a doped polycrystalline layer containing a lattice to the substrate and annealing the doped polycrystalline layer with a laser to incorporate the at least one dopant element into the lattice.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the

appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0011] Figures 1A-1E depict a step-wise formation of layers within a gate stack structure;

[0012] Figure 2 is a flow chart illustrating a process to deposit a doped polysilicon layer within a gate stack; and

[0013] Figures 3A-3C depict formation of layers within a gate stack structure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0014] The present invention teaches methods for forming a doped polycrystalline silicon layer onto a dielectric material, such as silicon dioxide, silicon oxynitride or a high dielectric constant material. Generally, the polycrystalline layer is doped by ion implantation, thermally annealed, such as with a rapid thermal annealing (RTA) process, and subsequently laser annealed to activate the dopants by a dynamic surface anneal (DSA) process.

[0015] Figures 1A-1E show a cross-sectional view of a gate stack structure progressing through processes disclosed in the present invention. Figure 1A depicts a dielectric layer 20 disposed on a substrate 10, such as a silicon substrate used in semiconductor processes. In one example, substrate 10 may be a 300 mm p-type silicon substrate doped with boron to resistivity from about 15 Ω-cm to about 20 Ω-cm and is usually pre-cleaned with a conventional pre-gate clean prior to the deposition of dielectric layer 20.

[0016] Dielectric layer 20 may be deposited to substrate 10 by a variety of deposition processes, such as rapid thermal oxidation (RTO), chemical vapor deposition (CVD), plasma enhanced-CVD (PE-CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), atomic layer epitaxy (ALE) or combinations thereof. Preferably, a dielectric material, such as SiO_2 or SiO_xN_y, is grown on the

substrate 10 by an RTO process. Materials suitable as dielectric layer 20 include silicon oxide, silicon nitride, silicon oxynitride, hafnium oxide, hafnium silicate, aluminum oxide, aluminum silicate, zirconium oxide, zirconium silicate, derivatives thereof and combinations thereof. Generally, dielectric layer 20 is deposited with a thickness from about 1 Å to about 150 Å, preferably from about 5 Å to about 50 Å.

[0017] In some embodiments, the dielectric material may be nitrided, such as with decoupled plasma nitridation (DPN) or thermal nitridation in nitric oxide (NO) or nitrous oxide (N_2O). A post-nitridation anneal is conducted to more strongly bond nitrogen into the oxide and to improve the interface between dielectric layer 20 and the substrate 10. For example, silicon oxide may be grown to substrate 10 by an RTO process, followed by a DPN process to form a silicon oxynitride with a nitrogen concentration from about $1x10^{14}$ atoms/cm^2 to about $1x10^{16}$ atoms/cm^2, for example, about $1x10^{15}$ atoms/cm^2. Other nitrided dielectric materials include aluminum oxynitride, nitrided hafnium silicate, hafnium oxynitride and zirconium oxynitride.

[0018] In Figure 2, a flow chart depicts process 100 including step 110 to deposit polysilicon layer 30, such as polycrystalline silicon, to the dielectric layer 20, as shown in Figure 1B. Polysilicon layer 30 is generally deposited by chemical vapor deposition (CVD), rapid thermal-CVD (RT-CVD), plasma enhanced-CVD (PE-CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), atomic layer epitaxy (ALE) or combinations thereof. Preferably, the polysilicon layer 30 is deposited with an RT-CVD process at a temperature from about 650°C to about 800°C, and more preferably from about 700°C to about 750°C. During an RT-CVD process, the temperature may be varied to induce variances in grain size of the polysilicon layer 30. For example, the average polysilicon grain size may be about 50 Å larger at 720°C than at 710°C. Generally, polysilicon layer 30 is deposited with a thickness from about 100 Å to about 10,000 Å, preferably from about 500 Å to about 2,500 Å, and more preferably from about 750 Å to about 1,500 Å. Beside grain sizes, dual layer polysilicon also can be deposited with RT-CVD technique. Polysilicon layer 30 is generally polycrystalline silicon, but may contain other elements such as germanium and or carbon. Therefore, polysilicon layer 30 may include Si, SiGe, SiC

or SiGeC. In some embodiments, the polysilicon layer may have a columnar structure with thin diameter or a dual layer structure combination including a micrograin layer on the bottom and a columnar layer on the top.

[0019] Hardware that may be used to deposit dielectric layers and/or polysilicon layers include the Epi Centura® system and the PolyGen® system available from Applied Materials, Inc., located in Santa Clara, California. A useful rapid-thermal CVD chamber for growing oxides is the Radiance® system available from Applied Materials, Inc., located in Santa Clara, California. An ALD apparatus that may be used to deposit high-k layers and/or polysilicon layers is disclosed in commonly assigned United States Patent Publication Number 20030079686, and is incorporated herein by reference in entirety for the purpose of describing the apparatus. Other apparatuses include batch, high-temperature furnaces, as known in the art.

[0020] Step 120 includes the doping of polysilicon layer 30 with elemental dopants 31. Figure 1C illustrates elemental dopants 31 in an upper portion 32 of polysilicon layer 30. The elemental dopants penetrate into the upper portion 32 of polysilicon layer 30 at a depth from about a single atomic layer to about 150 Å, preferably at about 70 Å. Elemental dopants may include boron, arsenic, phosphorus, gallium, antimony, indium or combinations thereof. Elemental dopants may have a concentration in the polysilicon layer 30 from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3. For example, polysilicon layer 30 is doped P type, such as by using boron ions to add boron at a concentration in the range from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3, preferably from about 1×10^{20} atoms/cm^3 to about 5×10^{20} atoms/cm^3. In another example, polysilicon layer 30 is doped N^+ type, such as by ion implanting of phosphorus to a concentration in the range from about 1×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3, preferably from about 1×10^{20} atoms/cm^3 to about 5×10^{20} atoms/cm^3. In another example, polysilicon layer 30 is doped N^- type, such as by diffusion of arsenic or phosphorus to a concentration in the range from about 1×10^{15} atoms/cm^3 to about 1×10^{19} atoms/cm^3.

[0021] Dopants may be implanted with an ion implantation process, such as described in commonly assigned, United States Patent No. 6,583,018, which is incorporated herein by reference in entirety for the purpose of describing the apparatus. An ion implantation apparatus useful during this embodiment is capable of ion implantation at a very low implantation energy of about 5 KeV or less, preferably about 3 KeV or less. Two ion implantation apparatuses useful in the present invention are manufactured and sold under the names Quantum III® system and Implant xR LEAP® system, both available from Applied Materials Inc., Santa Clara, California. For example, boron is implanted with energy of about 3 KeV and a dose from about 1×10^{15} atoms/cm^2 to about 1×10^{14} atoms/cm^2. In one example, the boron is implanted at about 4×10^{15} atoms/cm^2. In another example, boron is implanted at about 8×10^{15} atoms/cm^2.

[0022] In step 130, the substrate is exposed to a thermal anneal process to diffuse and distribute the dopant elements 31 from the upper portion 32 throughout the polysilicon layer 30 to form a doped polysilicon layer 34. The preferred annealing process is a rapid thermal annealing (RTA) process lasting from about 2 seconds to about 20 seconds, preferably from about 5 seconds to about 10 seconds. The RTA process heats the substrate to a temperature from about 800°C to about 1,400°C, preferably from about 1,000°C to about 1,200°C. For example, an RTA process heats the substrate to about 1,000°C for about 5 seconds. The correct combination of temperature and time ensures that the RTA process distributes elemental dopants 31 throughout the polysilicon layer 30 without contaminating nearby features in the device, as depicted in Figure 1D. One RTA chamber that has been found to be useful is the Centura RTP® system available from Applied Materials, Inc., located in Santa Clara, California.

[0023] In step 140, the doped polysilicon layer 34 was laser annealed by a dynamic surface annealing (DSA) process. The DSA process activates the elemental dopants 31 and the silicon within the doped polysilicon layer 34 to form an activated-doped polysilicon layer 36, as depicted in Figure 1E. The activation replaces atom sites from the crystalline lattice of a polysilicon layer with dopant

atoms 33. Therefore, the crystalline lattice, usually silicon, opens and incorporates the incoming dopant atoms 33, such as boron, arsenic, phosphorus or other dopants previously disclosed.

[0024] The DSA process heats the doped polysilicon layer 34 near the melting point, without actually causing a liquid state. The DSA process heats the doped polysilicon layer 34 to a temperature from about 1,000°C to about 1,415°C, preferably from about 1,050°C to about 1,400°C. Temperatures higher than the melting point of polycrystalline silicon (1,415°C) are not desirable, since dopant diffusion is likely to cause contamination of other materials within the feature. Depending on temperature, the substrate is exposed to the laser for various time durations. The DSA process is conducted for less than 500 milliseconds, preferably less than 100 milliseconds. The DSA process may be conducted on a DSA platform, available from Applied Materials, Inc., Santa Clara, California. Generally, the laser emits light with a wavelength selected from 10.6 μm or 0.88 μm.

[0025] Figures 3A-3C depicts the deposition of polysilicon during the formation of a gate stack structure. A dielectric layer 204 is deposed to a substrate 200, as shown with a cross-sectional view in Figure 3A. The substrate 200 may include, though not shown, a variety of features including doped regions. Dielectric layer 204 includes silicon dioxide, silicon oxynitride, silicon nitride and high-k materials as previously described. The substrate 200 also includes shallow trench isolations (STIs) 202. STIs 202 are generally formed by oxidizing the sidewalls of trenches etched into substrate 200 and subsequent filling of the trenches with a high desity plasma CVD oxide.

[0026] Figure 3B illustrates polysilicon layer 206 deposited on the dielectric layer 204 and the STI 202. Polysilicon layer 206 may be deposited by chemical vapor deposition (CVD), rapid thermal-CVD (RT-CVD), plasma enhanced-CVD (PE-CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), or combinations thereof. In one embodiment, polysilicon layer 206 is deposited with an RT-CVD process at a temperature from about 650°C to about 800°C, and more preferably

from about 700°C to about 750°C. Generally, polysilicon layer 206 is deposited with a thickness from about 100 Å to about 10,000 Å, preferably from about 500 Å to about 2,500 Å, and more preferably from about 750 Å to about 1,500 Å. Polysilicon layer 206 is generally polycrystalline silicon, but may contain other elements such as germanium and or carbon. Therefore, polysilicon layer 206 may include Si, SiGe, SiC or SiGeC.

[0027] Polysilicon layer 206 is patterned and etched to form a patterned polysilicon 208, as depicted in Figure 3C. Polysilicon layer 206 may be doped prior to being etched, but generally is maintained undoped until patterned polysilicon 208 is formed. Patterned polysilicon 208 may be doped, annealed and/or have more layers deposited thereon, such as an offset spacer (not shown). For example, patterned polysilicon may be encapsulated with the deposition of an offset spacer and subsequently doped with an ion implantation process, exposed to a RTA process to anneal and exposed to a DSA process to activate the implanted dopants.

Experiments

[0028] To simulate a doped polycrystalline silicon gate electrode, polycrystalline silicon was deposited on eight substrates (Substrates A-H) containing a layer of silicon oxynitride gate dielectric, as shown in Table 1. The substrates were 300 mm p-type (boron doped) silicon wafers with resistivity of 15-20 Ω-cm. The substrates were exposed to a pre-gate clean, followed by exposure to a rapid thermal oxidation process. A SiO_2 film was formed with a thickness of about 20 Å. The SiO_2 film was plasma nitrided by decoupled plasma nitridation, resulting in a nitrogen concentration of about $1x10^{15}$ atoms/cm^2. All of the substrates were exposed to a post-nitridation anneal to more strongly bond nitrogen into the silicon oxide and improve the surface interface.

Substrate	Poly-Si (°C)	[B] ($\times 10^{15}$)	RTA	DSA
A	710	4	x	
B	710	4	x	x
C	720	4	x	
D	720	4	x	x
E	710	8	x	
F	710	8	x	x
G	720	8	x	
H	720	8	x	x

Table 1

[0029] Polycrystalline silicon was deposited with a single-wafer, rapid-thermal chemical vapor deposition tool to a thickness of about 1,000 Å. The average poly grain size was varied by depositing polysilicon at temperature of 710°C for Substrates A, B, E and F, while polysilicon was deposited to Substrates C, D, G and H at 720°C to produce larger grains. Boron was implanted with an energy of 3 KeV and a dose of $4\times10^{15}/cm^2$ to Substrates A-D and $8\times10^{15}/cm^2$ for Substrates E-H. All of the substrates went through a conventional RTA process at about 1,000°C. Substrates B, D, F and H were laser annealed by a DSA process at 1,350°C.

[0030] The sheet resistance (Rs) and spreading resistance of the resulting structures was measured to evaluate the carrier concentration and activation. The dopant (boron) profiles were analyzed by secondary ion mass spectroscopy (SIMS). Poly grain structure was analyzed with x-ray diffraction spectroscopy (XRD) and cross section transmission electron microscopy (TEM).

[0031] The laser anneal reduced the Rs greater than achieved by solely increasing the dopant concentration. For example, doubling the dopant concentration reduced Rs by about 10%. However, while maintaining the dopant concentration at $4\times10^{15}/cm^2$, the Rs was reduced as much as 40% for substrates exposed to a DSA process. The Rs was reduced as much as 50% on substrates

with doubled dopant concentration and exposed to a DSA process. Poly grain structure had little impact on the Rs. The polysilicon deposited at 720°C was a few percent lower in Rs then the polysilicon deposited at 710°C. Laser annealing reduced the sheet resistance through at least three mechanisms, such as additional dopant diffusion, alteration of the poly grain structure, and an increase in the dopant activation.

[0032] No additional dopant diffusion was observed by SIMS. The dopant was fully diffused by the RTA process, and no changes were seen after laser anneal. The laser irradiated each point on the wafer for only a few milliseconds, so the dopant did not have enough time to diffuse despite the high temperature. The polysilicon grain structure did show some minor changes with laser anneal. An XRD analysis showed that the grain size increased by 9 Å, from 361 Å to 370 Å after a DSA process. The TEM images showed that the columnar structures were well maintained, but grain structure appeared to be slightly more crystalline. Grain structure changes may have been a contributor to lower sheet resistance. However, there was no conspicuous increase in the grain size that would threaten device yield, as can occur with laser anneals above the silicon melting temperature.

[0033] The spreading resistance profiles showed that the carrier concentration increased with the laser anneal temperature throughout the polysilicon. The dopant activation increase was particularly large at the interface between the polysilicon and the oxynitrided layer. The higher carrier concentration reduced the poly-depletion. Laser annealing may have reduced the sheet resistance through an increase in dopant activation. The brief, high temperature laser anneal created more carriers in the polysilicon film.

[0034] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.